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Title: IMAGE DISPLAY APPARATUS

(Partial Translation: From Page 2 (-552-) lower right column, line 1 to Page 3 (-553-) upper right column, line 9)

Fig. 2 is a circuit diagram of an active matrix type image display apparatus according to an embodiment of the invention. The embodiment will be described assuming that the liquid crystal is used as the display element and the field effect transistor is used as the switching element.

In Fig. 2, SA_0 to SA_m represent the source line, GA_1 to GA_n represent the source line, $UA_{1,1}$ to $UA_{n,m}$ represent the pixel circuit, and $T_{1,1}$ to $T_{n,m}$ and $R_{2,1}$ to $R_{n,m}$ represent the field effect transistor. Similarly to Fig. 1, UU represents the integration of the capacitor and the pixel electrode.

The feature of the invention is that all the pixel circuits except for the pixel circuits ($UA_{1,1}$ to $UA_{1,m}$) belonging to the first line have two field effect transistors and the pixel circuits belonging to the odd-number line differs from the pixel circuits belonging to the even-number line in the connection of the field effect transistor and the source line and the gate line. For example, in the pixel circuit $UA_{2,1}$ belonging to the even-number line, the gate terminal of the field effect transistor $R_{2,1}$ is connected to the gate line GA_1 and the input terminal of the field effect transistor $R_{2,1}$ is connected to the source line SA_1, and the gate terminal of the field effect transistor $T_{2,1}$ is

connected to the gate line GA_2 and the input terminal of the field effect transistor $T_{2,1}$ is connected to the source line SA_0.

On the other hand, in the pixel circuit $UA_{3,1}$ belonging to the odd-number line, the gate terminal of the field effect transistor $R_{3,1}$ is connected to the gate line GA_2 and the input terminal of the field effect transistor $R_{3,1}$ is connected to the source line SA_0, and the gate terminal of the field effect transistor $T_{3,1}$ is connected to the gate line GA_3 and the input terminal of the field effect transistor $T_{3,1}$ is connected to the source line SA_1. Although it is possible that the pixel circuit absolutely similar to the pixel circuits from the second line is used as the first-line pixel circuit, here, the use of the pixel circuit including one field effect transistor will be described.

With reference to Fig. 2, the action of the invention will be described below. The data signals to be input to the pixel circuits $UA_{1,1}$ to $UA_{1,m}$ are applied to the source lines SA_1 to SA_m. Then, voltage is applied to the gate line GA_2 to make the field effect transistors $T_{2,1}$ to $T_{2,m}$ an "on" state, and the data signals are written in the capacitors in the pixel circuits. In parallel with the above-described action, the field effect transistors $R_{2,2}$ to $R_{2,m}$ become the "on" state, and the data signals are also written in the capacitors in the pixel circuits $UA_{2,1}$ to $UA_{2,m}$. After the write is sufficiently performed, the voltage applied to the gate line GA_1 is removed, and the capacitors in the pixel circuits retain the data signals. Then, the data signals to be input to the pixel circuits $UA_{2,1}$ to $UA_{2,m}$ are applied to the source lines SA_0 to SA_{m-1}, and the pixel circuits $UA_{2,1}$ to $UA_{2,m}$ and the pixel circuits $UA_{3,1}$ to $UA_{3,m}$ similarly retain the data signals. The data signals to be input to each of the pixel circuits are retained by sequentially repeating the similar action, and the liquid crystal is driven by the pixel electrodes which become the potential corresponding to the data signal.

Fig. 1

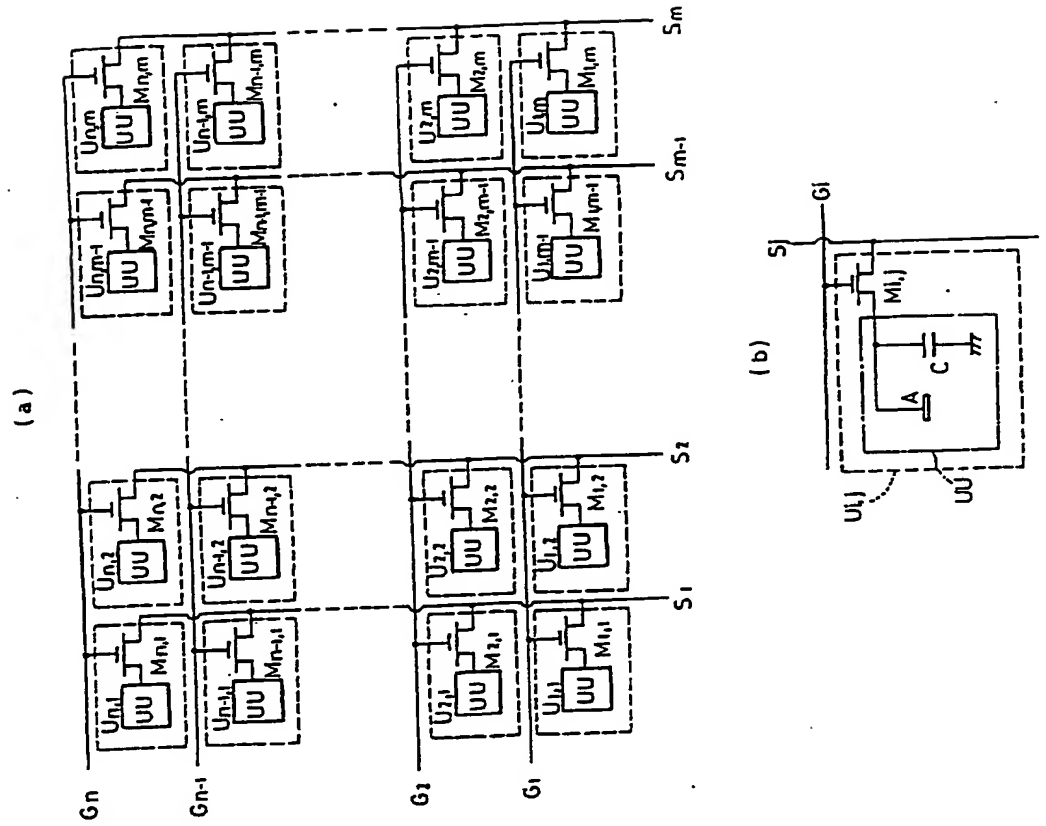

(a)
(b)
Sm
Sm-1
S2
S1
Gn
Gn-1
G2
G1
Gj
Sj
Mi,j
A
C
Ui,j
UU

Fig. 2

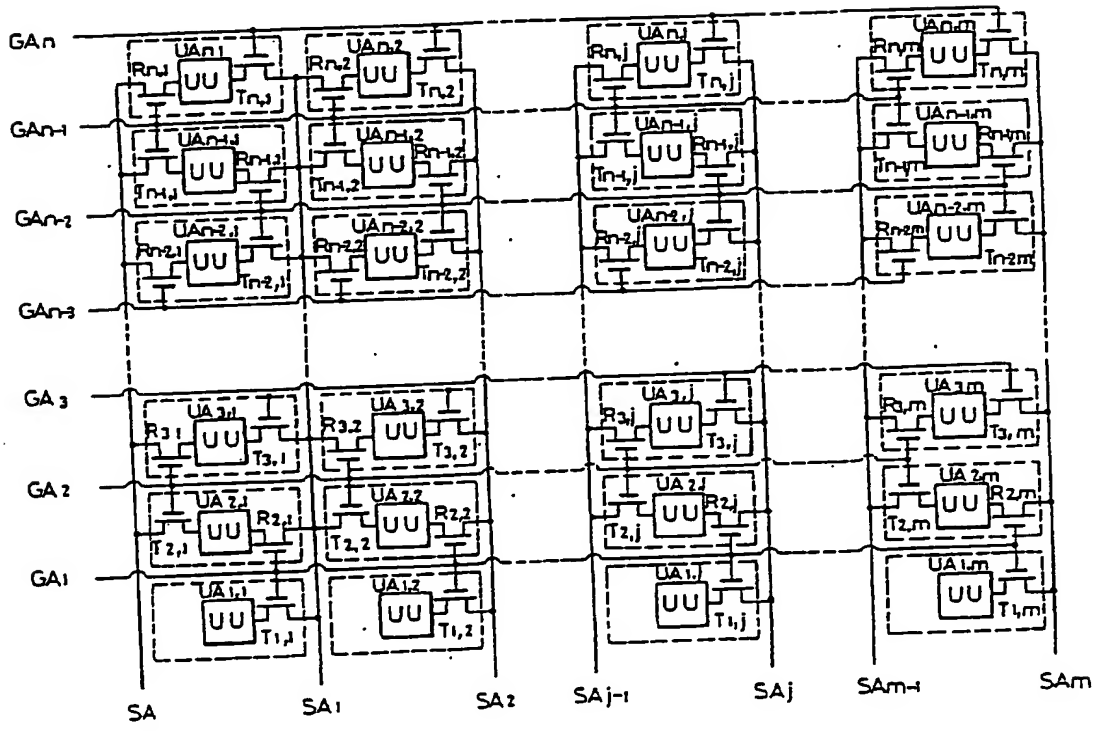
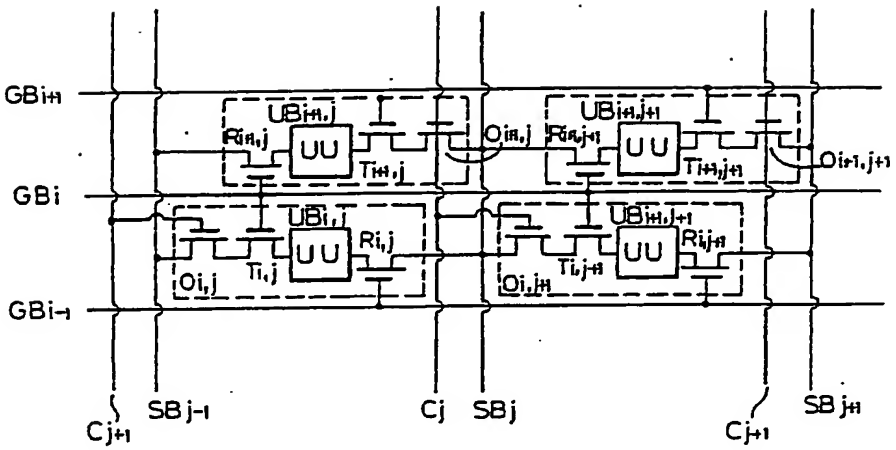

GAn
GAn-1
GAn-2
GAn-3
GA3
GA2
GA1
SA
SA1
SA2
SAj-1
SAj
SAm-1
SAm

Fig. 3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Ri+1,j
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Ti+1,j
Oi+1,j
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Oi+1,j+1
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